

**LISTING OF THE CLAIMS**

The following is a complete listing of the claims with a status identifier in parenthesis.

**LISTING OF CLAIMS**

1. (Cancelled).
  
2. (Previously Presented) A circuit arrangement for a reception part of an SDH (=Synchronous Digital Hierarchy) transmission system for transmitting plesiochronous signals, comprising:
  - a clock synchronizer receiving the plesiochronous signals through a plurality of input channels allocated to the plesiochronous signals and adapting the received plesiochronous signals to a common processing clock, the clock synchronizer including a plurality of buffer memories corresponding to the plurality of input channels for writing in the plesiochronous signals with their plesiochronous signal clock, and for reading out the signals with a synchronous processing clock;
  - a reception multiplexer for receiving the signals with the synchronous processing clock;
  - a reception processing means connected at an output of the reception multiplexer for transforming a plesiochronous signal into a synchronous signal for an SDH transmission channel; and
  - a demultiplexer following the reception-processing means.

3. (Cancelled)
4. (Original) A circuit arrangement for a transmission part of an SDH transmission system for transmitting plesiochronous signals, comprising:
  - a transmission multiplexer, at the output of which a transmission processing means for transforming a transmitted synchronous signal into a plesiochronous signal is connected, and
  - a desynchronizer following the transmission processing means for recovery of the plesiochronous signal clocks of the plesiochronous signals and to issue the plesiochronous signals to a plurality of output channels.
5. (Original) The circuit arrangement of Claim 4, wherein the transmission processing means is connected to a transmission demultiplexer contained in the desynchronizer.

6. (Previously Presented) The circuit arrangement of Claim 2, wherein the reception processing means comprises:

a synchronizer for equalizing the bit rates of the plesiochronous signal;  
and

a mapper for mapping the equalized plesiochronous signal to provide the synchronous signal.